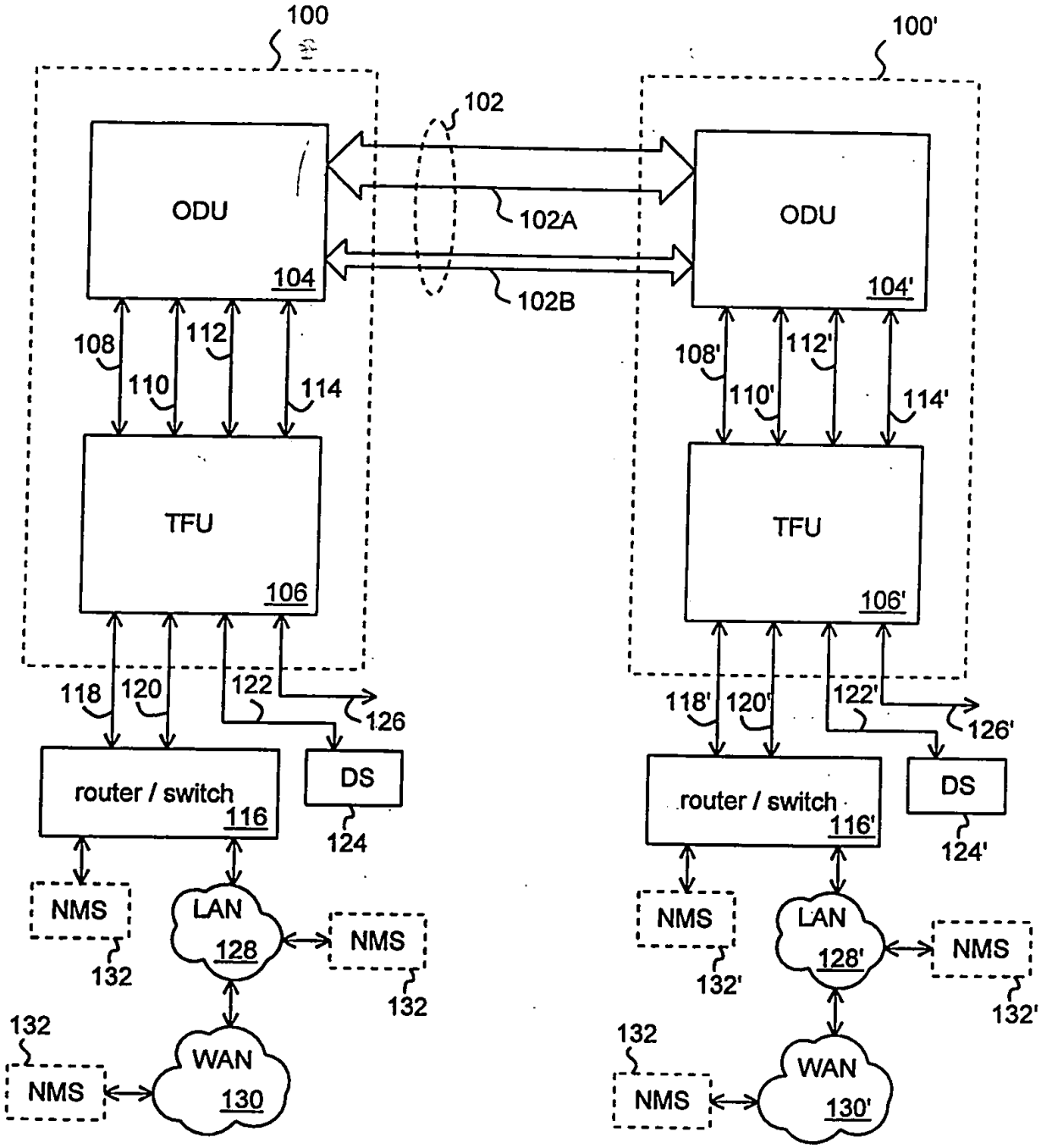

100
100'
102
ODU
104
102A
102B
ODU
104'
108
110
112
114
108'
110'
112'
114'
TFU
106
TFU
106'
118
120
122
126
118'
120'
122'
126'
router / switch
116
DS
124
router / switch
116'
DS
124'
NMS
132
LAN
128
NMS
132
NMS
132'
LAN
128'
NMS
132'
132
NMS
WAN
130
132
NMS
WAN
130'

Fig. 1

Fig. 2A

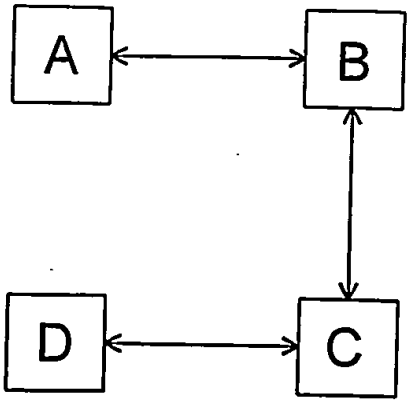


Fig. 2B

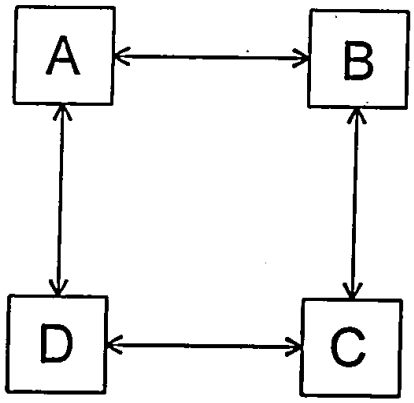


Fig. 2C

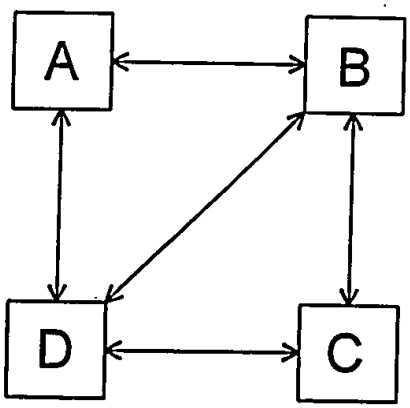


Fig. 2D

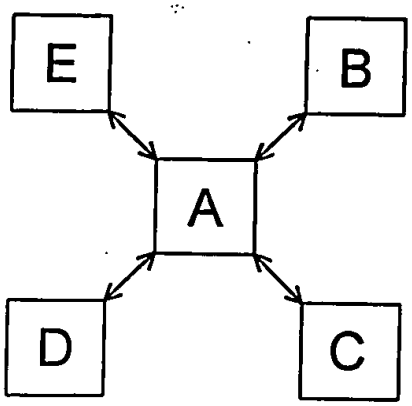


Fig. 2E

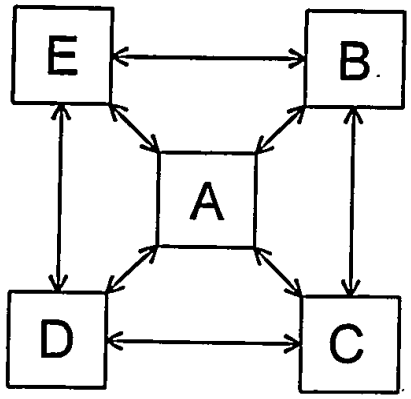


Fig. 2F

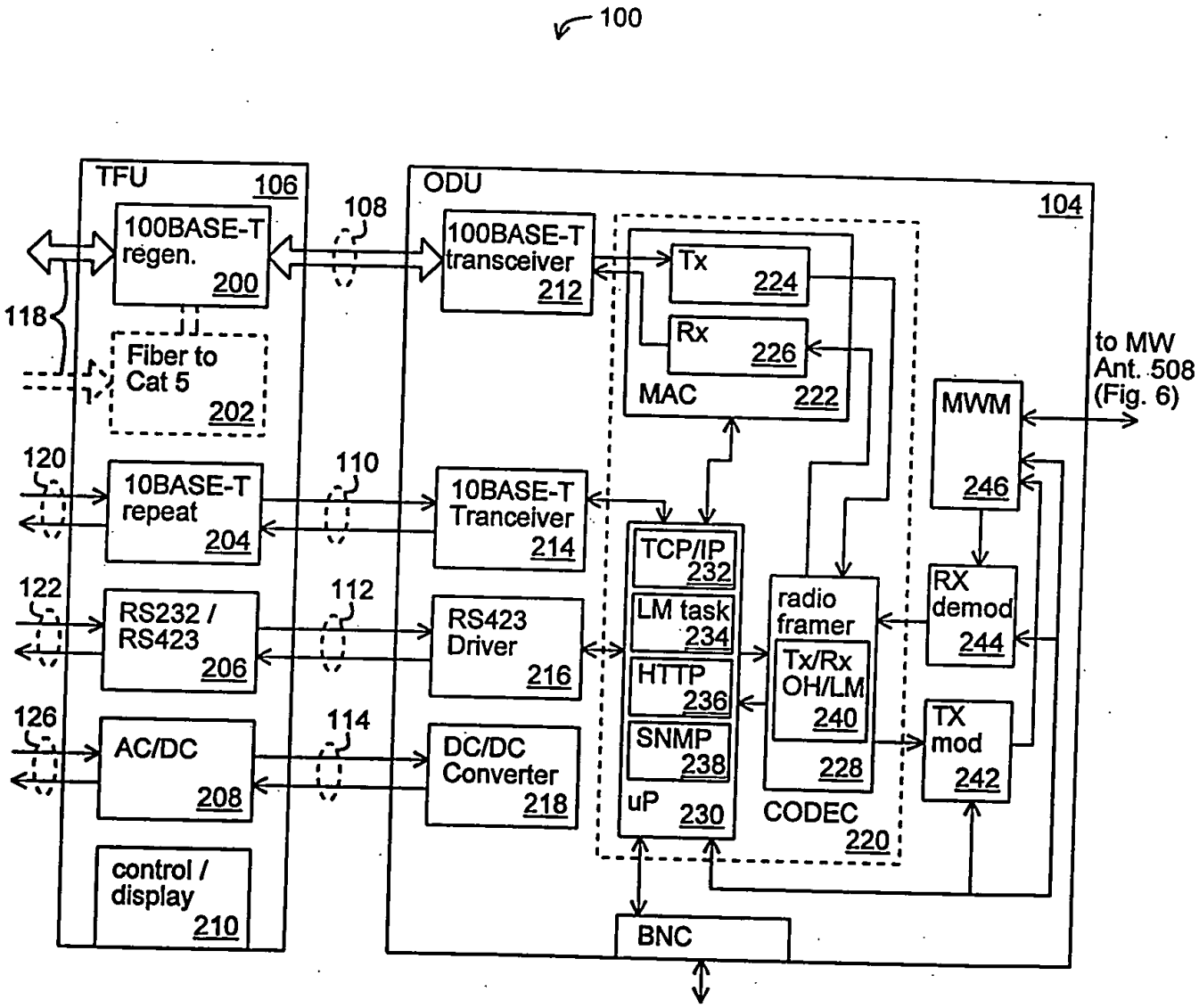

100
TFU
106
ODU
104
100BASE-T regen.
200
108
100BASE-T transceiver
212
Tx
224
Rx
226
MAC
222
118
Fiber to Cat 5
202
to MW Ant. 508 (Fig. 6)
MWM
246
120
10BASE-T repeat
204
110
10BASE-T Tranceiver
214
TCP/IP
232
LM task
234
HTTP
236
SNMP
238
uP
230
radio framer
Tx/Rx OH/LM
240
228
CODEC
220
RX demod
244
TX mod
242
122
RS232 / RS423
206
112
RS423 Driver
216
126
AC/DC
208
114
DC/DC Converter
218
control / display
210
BNC

Fig. 3

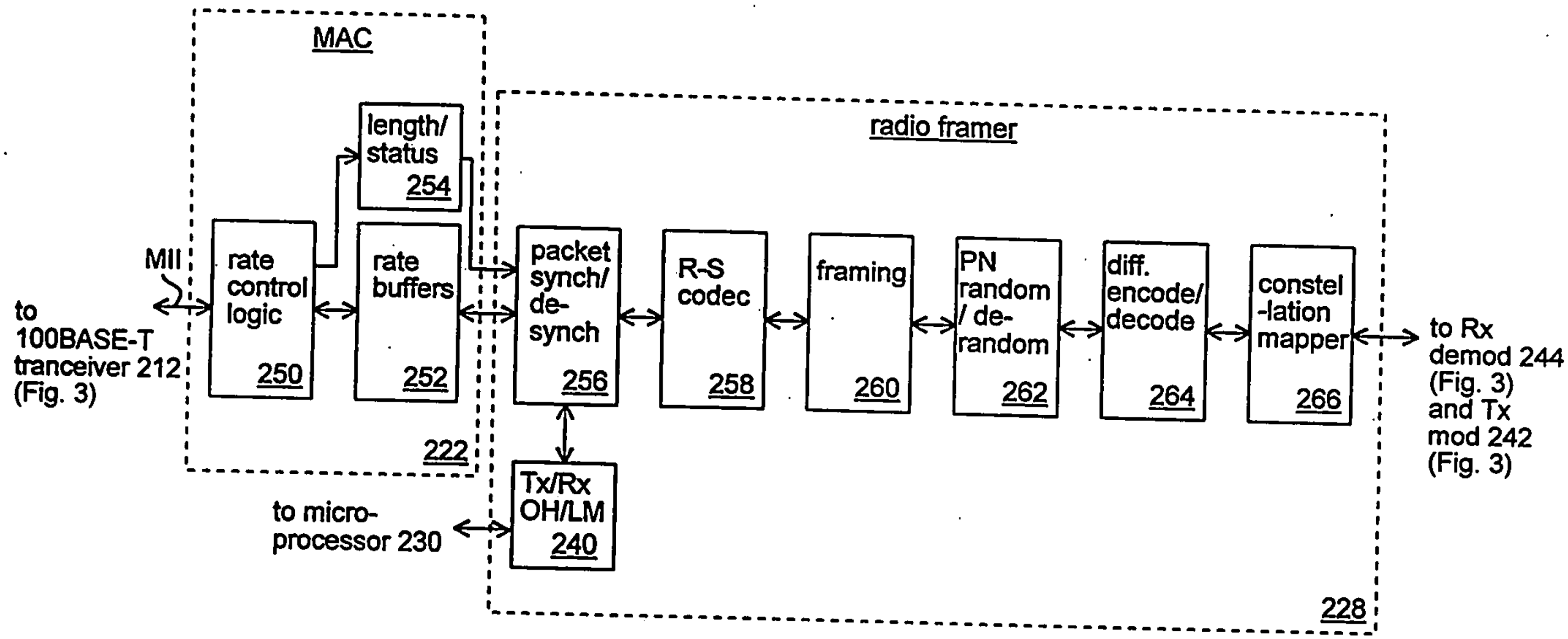

MAC
222
rate control logic
250
length/ status
254
rate buffers
252
radio framer
228
packet synch/ de-synch
256
R-S codec
258
framing
260
PN random / de-random
262
diff. encode/ decode
264
constel -lation mapper
266
Tx/Rx OH/LM
240
MII
to 100BASE-T tranceiver 212 (Fig. 3)
to micro-processor 230
to Rx demod 244 (Fig. 3) and Tx mod 242 (Fig. 3)

Fig. 4

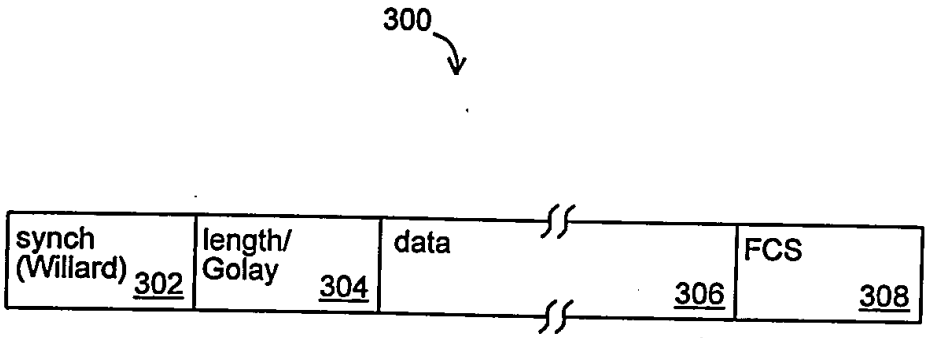


Fig. 5

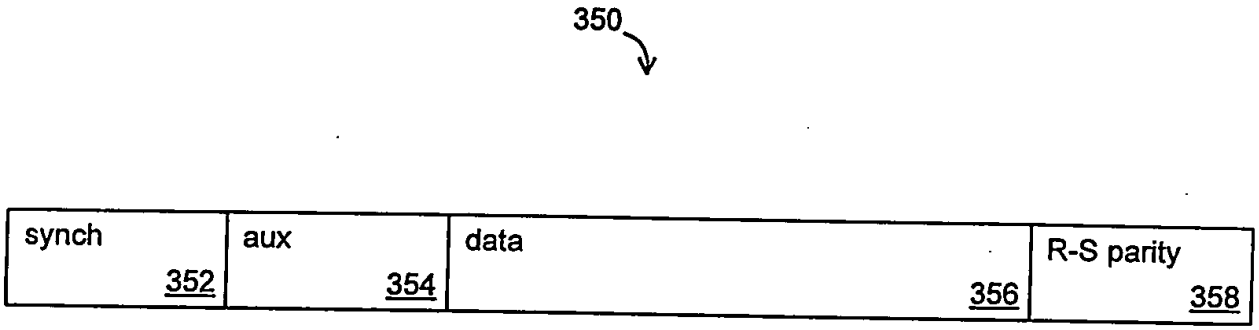


Fig. 6

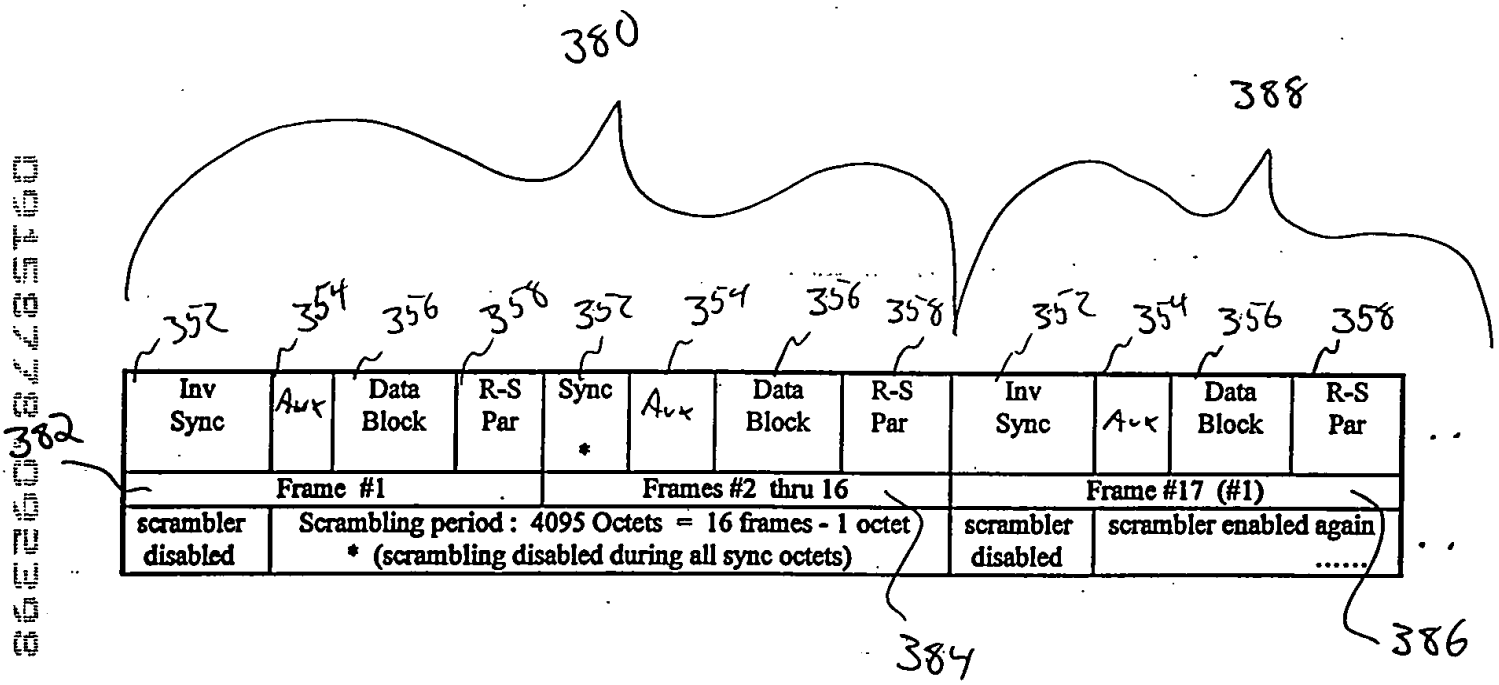

380
388
352
354
356
358
Inv Sync
Aux
Data Block
R-S Par
Sync *
382
Frame #1
Frames #2 thru 16
Frame #17 (#1)
scrambler disabled
Scrambling period : 4095 Octets = 16 frames - 1 octet
* (scrambling disabled during all sync octets)
scrambler enabled again
.....
384
386

Fig. 7

262

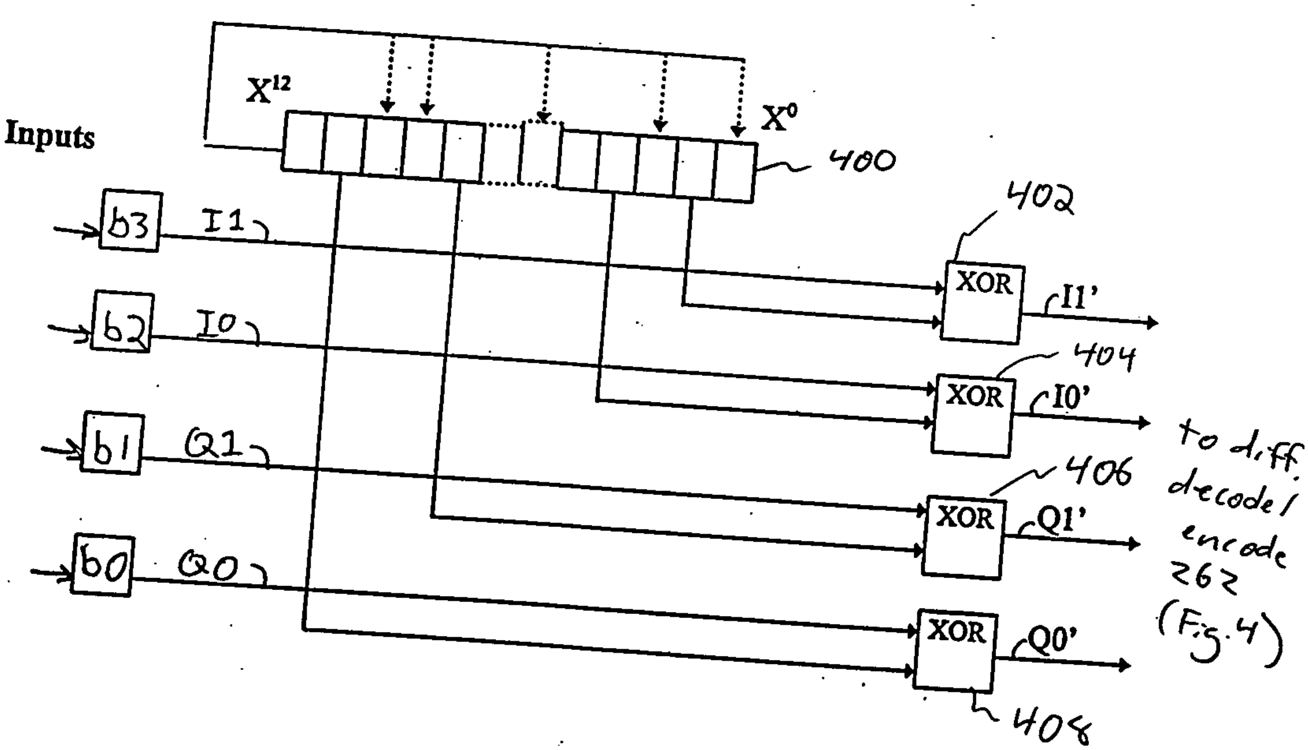


Fig. 8

```
Quad  = 2*I1' + Q1' ;        -- Map Quadrant Tag [0 1 2 3]
Phi   = [0 1 3 2] ;          --      to Angle = [0 1 3 2]
Angle = Phi(Quad)
Sum   = (Sum + Angle) modulo 4 ;
I1''  = bit 1 of Sum ;       I0''  = I0' ;
Q1''  = bit 0 of Sum ;       Q0''  = Q0' ;
```

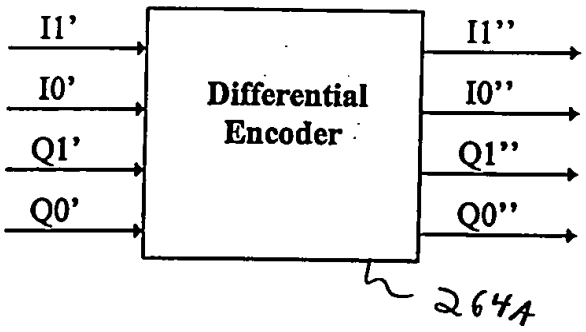


Fig. 9

Angle = 2*RxIs' + RxQs' ;
Phi' = [0 1 3 2] ;
Diff = (Phi'(Angle) - Phi_0) modulo 4 ;
Phi_0 = Phi'(Angle) ;
RxIs = bit 1 of Phi'(Diff) ;
TxIs = bit 0 of Phi'(Diff) ;

RxIm = RxIm' ;
RxQm = RxQm' ;

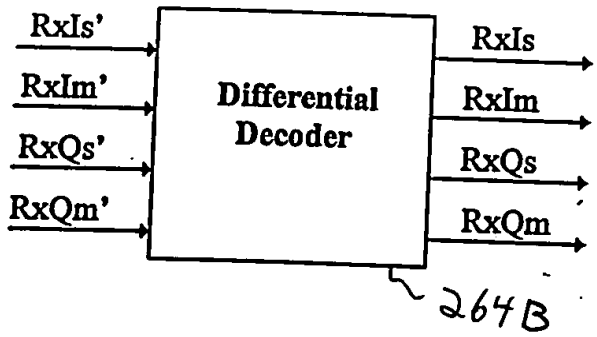


Fig. 10

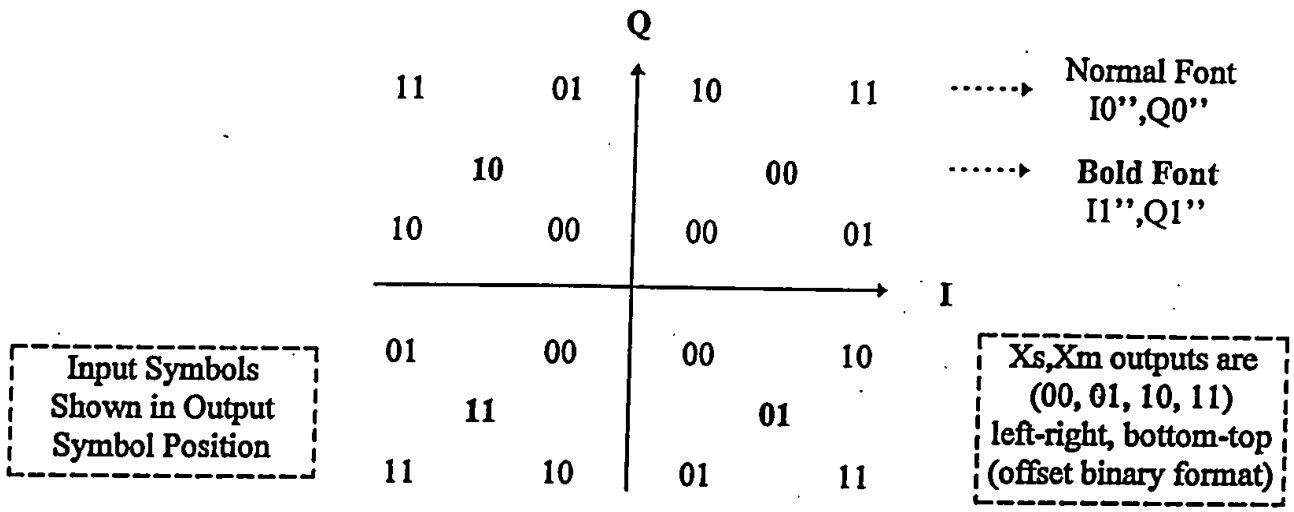

Q
I
11
01
10
11
10
00
10
00
00
01
01
00
00
10
11
01
11
10
01
11
Normal Font
I0'',Q0''
Bold Font
I1'',Q1''
Input Symbols
Shown in Output
Symbol Position
Xs,Xm outputs are
(00, 01, 10, 11)
left-right, bottom-top
(offset binary format)

Fig. 11

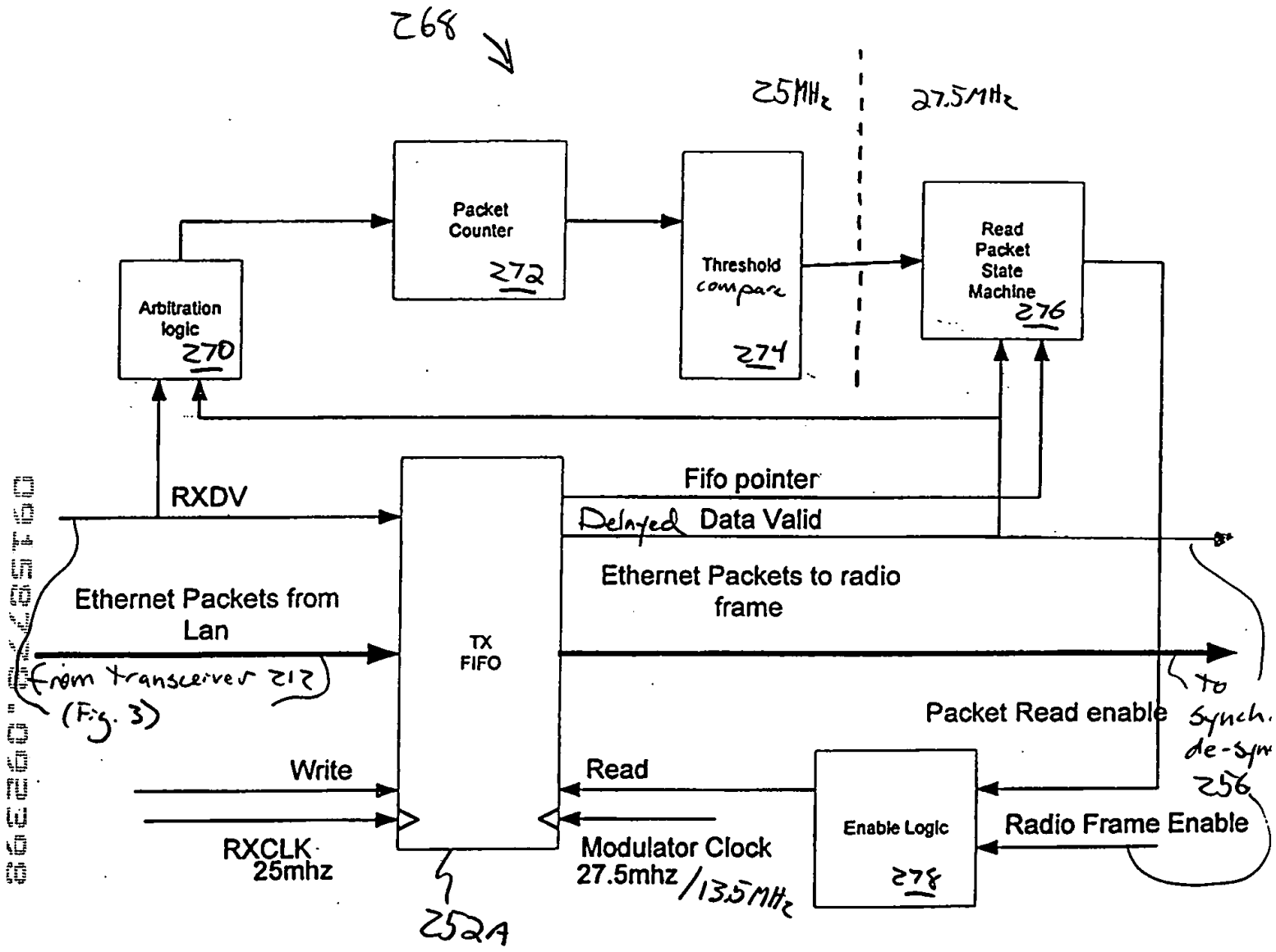

268
25MHz
27.5MHz
Packet Counter
272
Threshold compare
274
Read Packet State Machine
276
Arbitration logic
270
RXDV
Fifo pointer
Delayed Data Valid
Ethernet Packets to radio frame
Ethernet Packets from Lan
(from transceiver 212 (Fig. 3)
TX FIFO
To Synch. de-sync 256
Packet Read enable
Write
Read
Enable Logic
278
Radio Frame Enable
RXCLK 25mhz
Modulator Clock 27.5mhz/13.5MHz
252A

Fig. 12

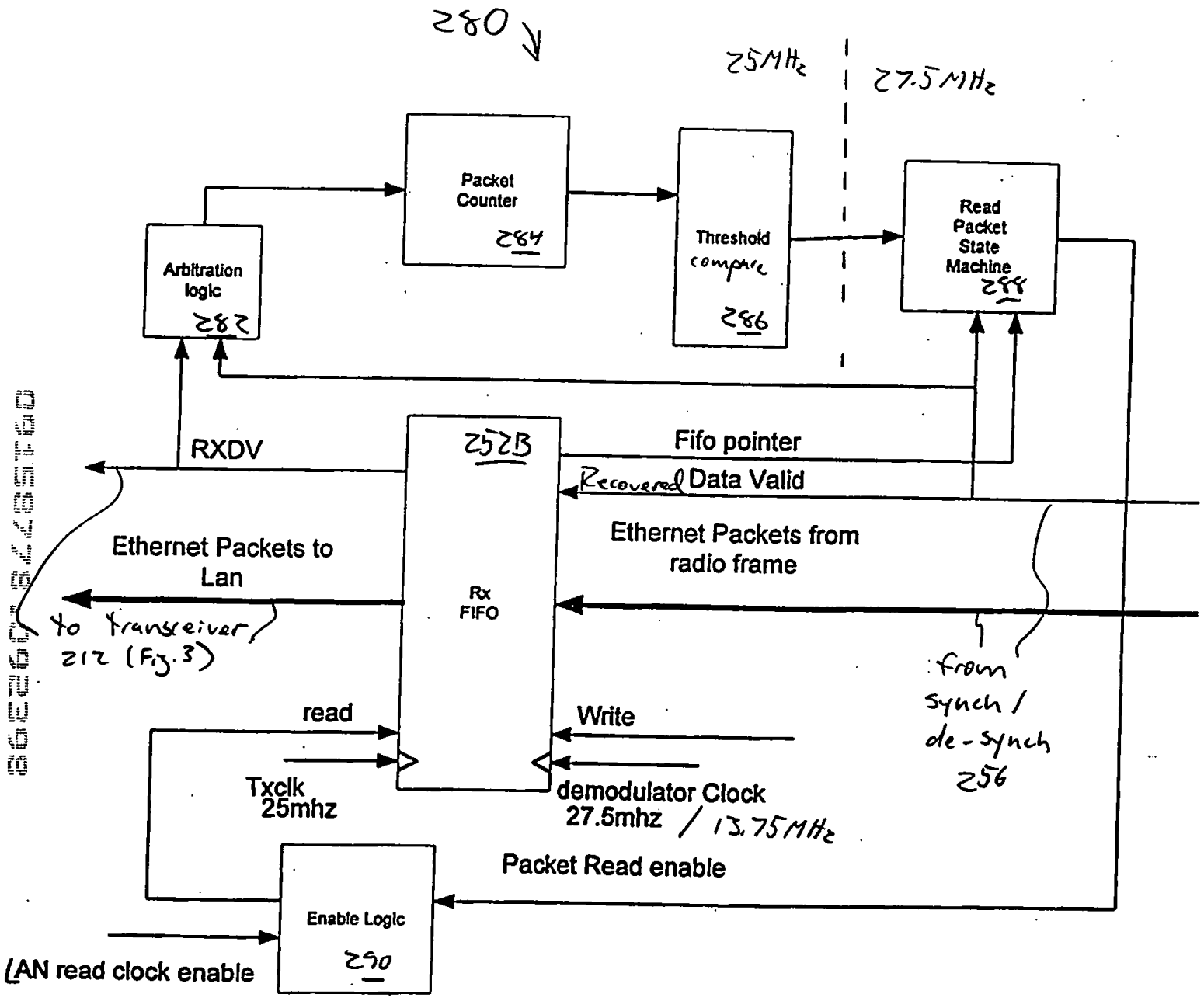

280
25MHz
27.5MHz
Packet Counter
284
Threshold compare
286
Read Packet State Machine
288
Arbitration logic
282
RXDV
252B
Fifo pointer
Recovered Data Valid
Ethernet Packets to Lan
Ethernet Packets from radio frame
Rx FIFO
to transceiver 212 (Fig. 3)
from synch / de-synch 256
read
Write
Txclk 25mhz
demodulator Clock 27.5mhz / 13.75MHz
Packet Read enable
Enable Logic
290
LAN read clock enable

Fig. 13

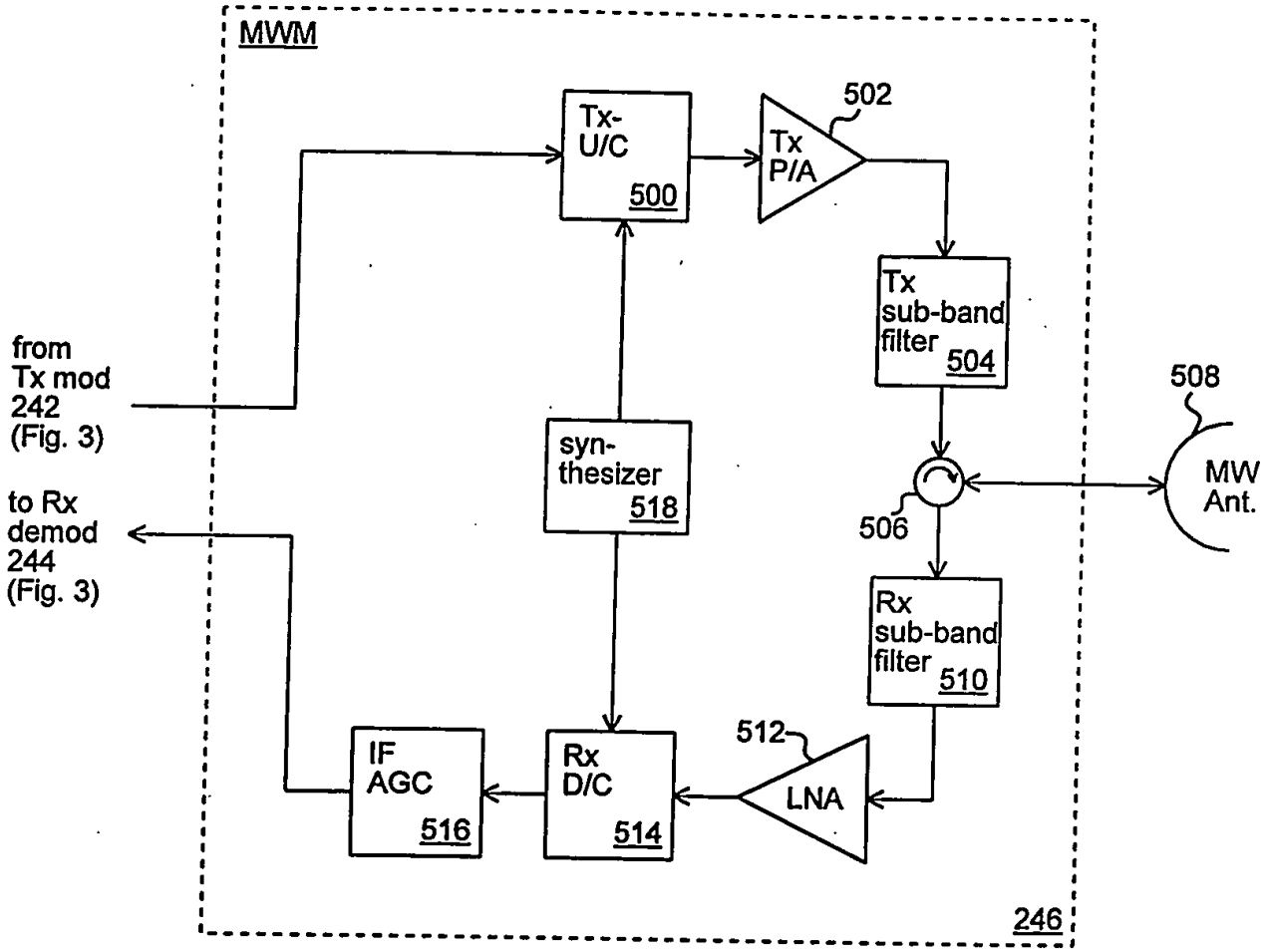

MWM
Tx-
U/C
500
502
Tx
P/A
Tx
sub-band
filter
504
508
MW
Ant.
from
Tx mod
242
(Fig. 3)
to Rx
demod
244
(Fig. 3)
syn-
thesizer
518
506
Rx
sub-band
filter
510
512
LNA
IF
AGC
516
Rx
D/C
514
246

Fig. 14

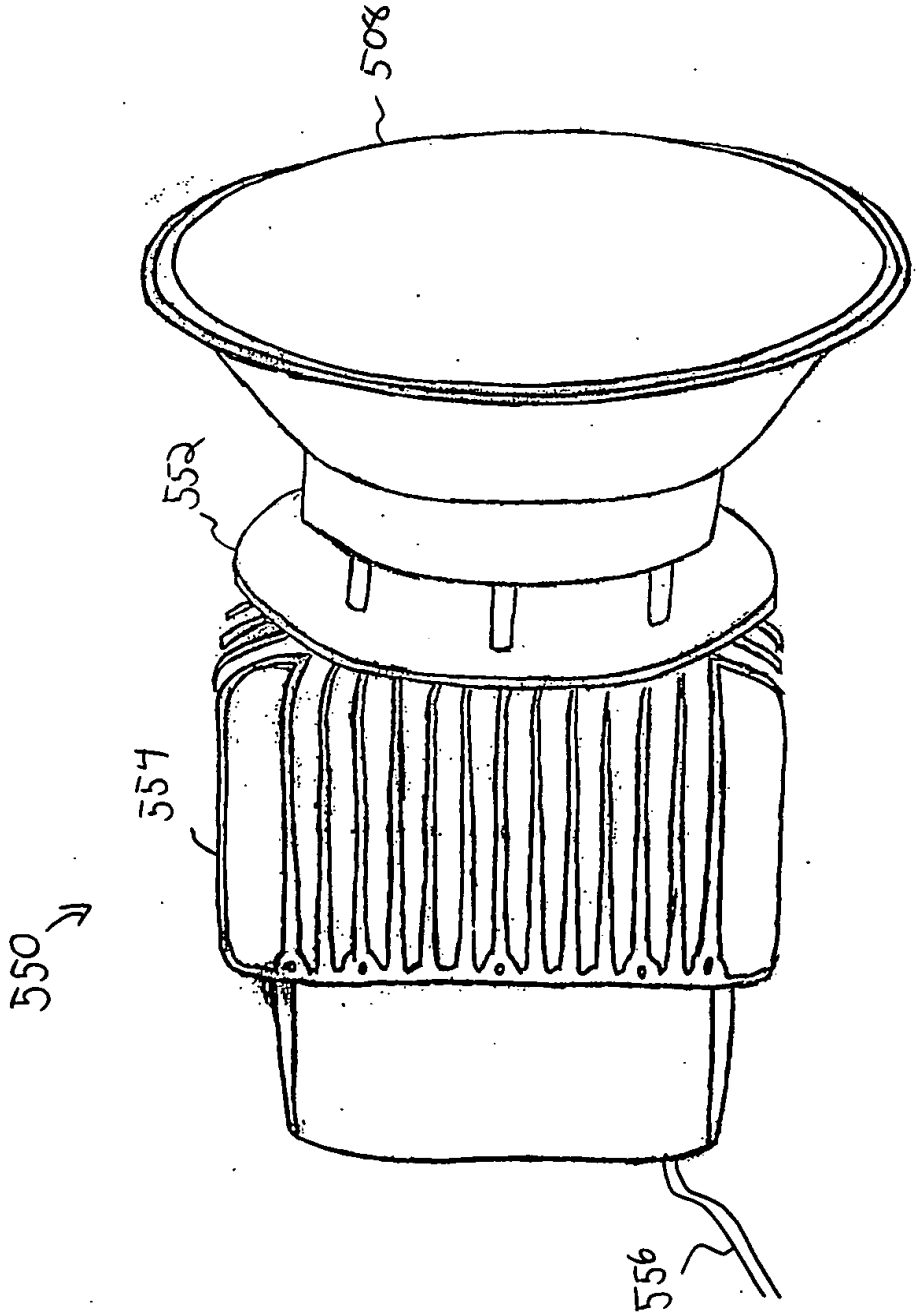


Fig. 15

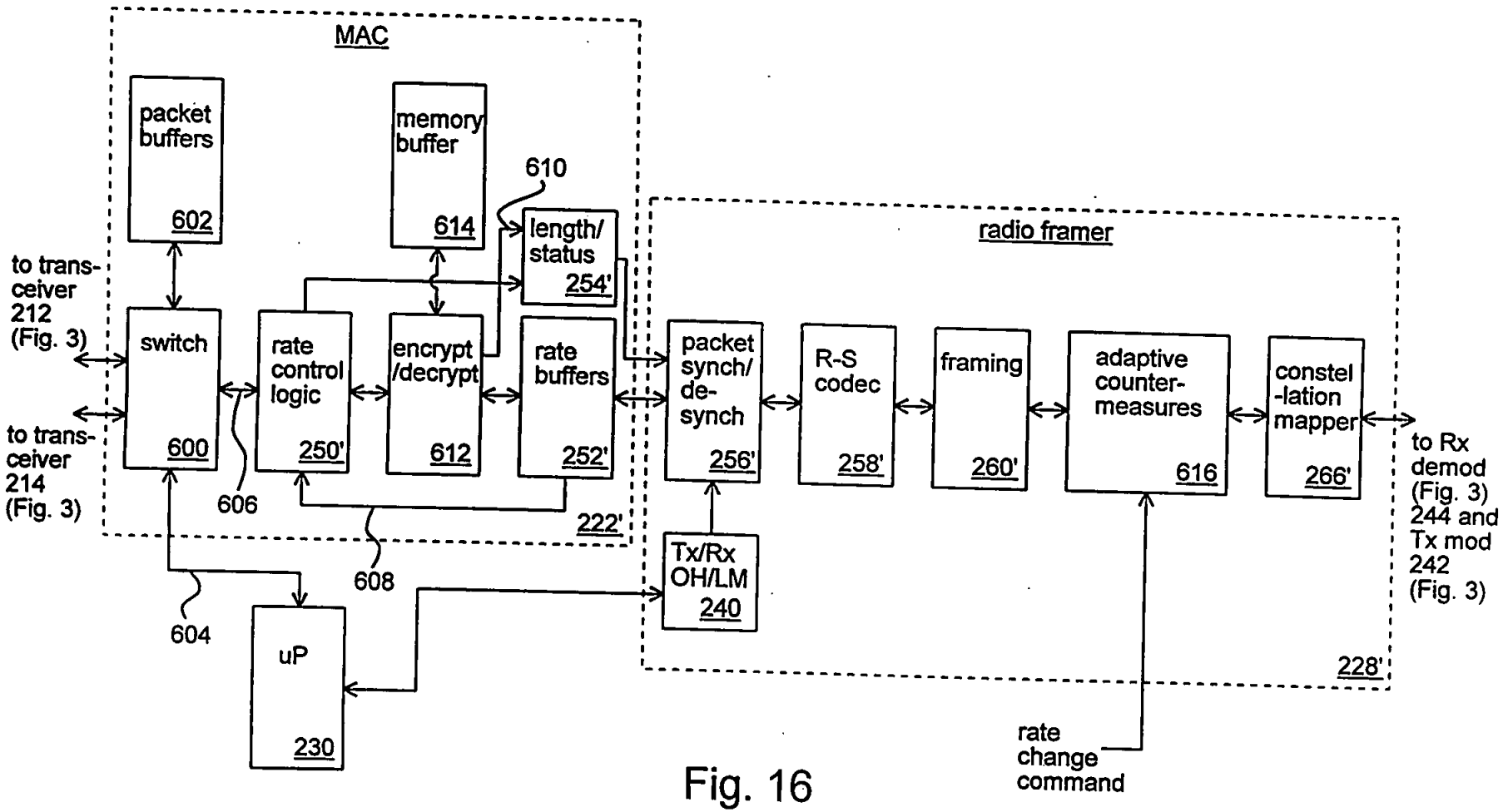

MAC
packet buffers
602
memory buffer
614
610
length/ status
254'
radio framer
to trans-ceiver 212 (Fig. 3)
switch
600
rate control logic
250'
encrypt /decrypt
612
rate buffers
252'
packet synch/ de-synch
256'
R-S codec
258'
framing
260'
adaptive counter-measures
616
constel -lation mapper
266'
to Rx demod (Fig. 3) 244 and Tx mod 242 (Fig. 3)
to trans-ceiver 214 (Fig. 3)
606
222'
608
604
Tx/Rx OH/LM
240
uP
230
228'
rate change command

Fig. 16

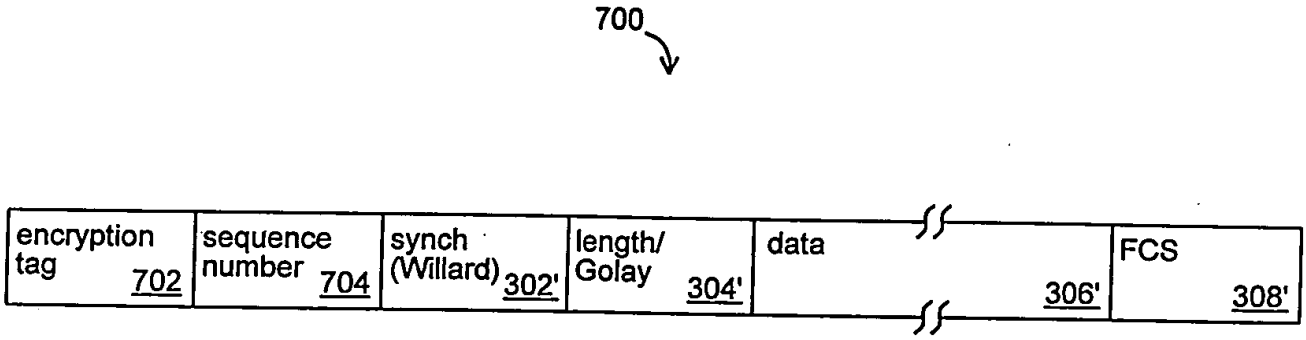
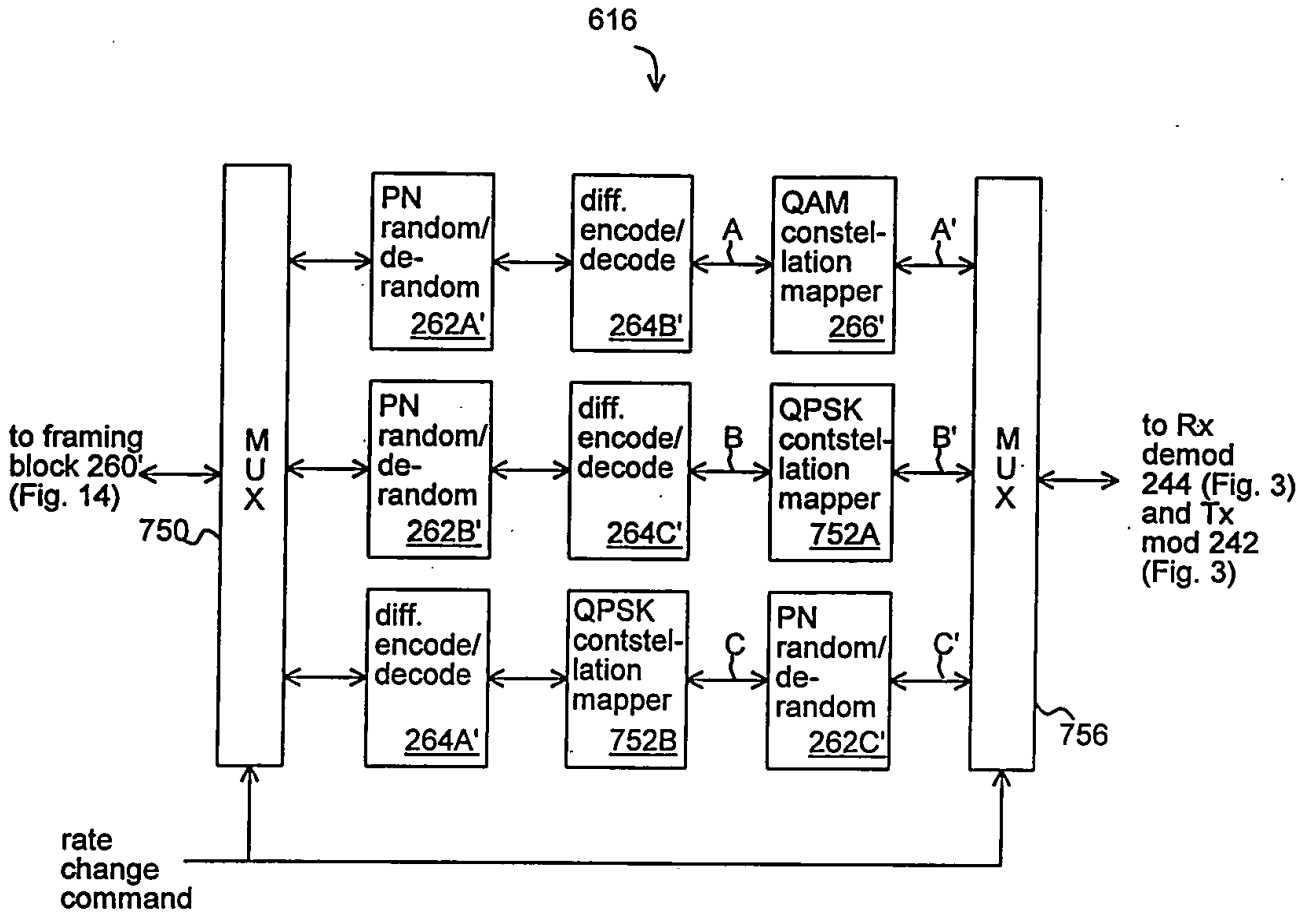

700
encryption tag 702
sequence number 704
synch (Willard) 302'
length/ Golay 304'
data 306'
FCS 308'

Fig. 17



A: data rate = 4 bits/symbol, symbol rate = 27.5 Msymbols (mega-symbols)/second

A': data rate = 4 bits/symbol, symbol rate = 27.5 Msymbols/second

B: data rate = 2 bits/symbol, symbol rate = 27.5 Msymbols/second

B': data rate = 2 bits/symbol, symbol rate = 27.5 Msymbols/second

C: data rate = 2 bits/symbol, symbol rate = 3.4375 Msymbols/second

C': data rate = 2 bits/symbol, symbol rate = 27.5 Msymbols/second

Fig. 18

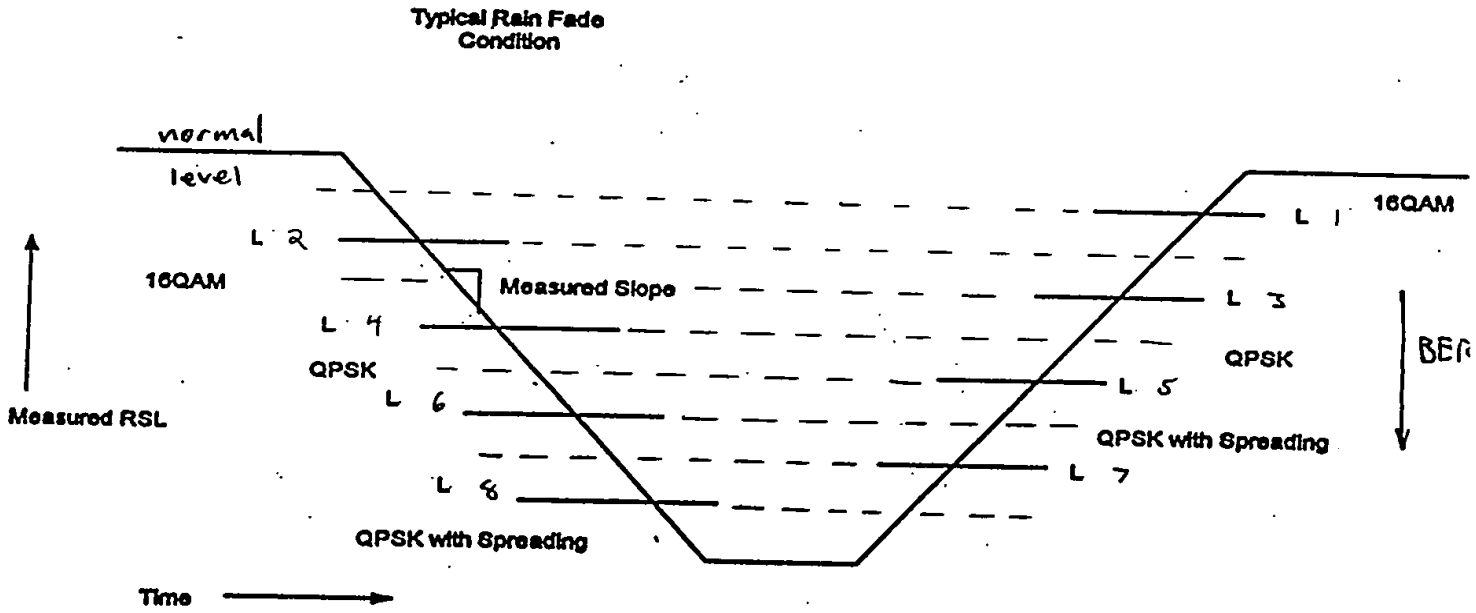

Typical Rain Fade Condition
normal level
L 2
16QAM
Measured Slope
L 4
QPSK
L 6
Measured RSL
L 8
QPSK with Spreading
Time
L 1
16QAM
L 3
QPSK
L 5
QPSK with Spreading
L 7
BER

Fig. 19

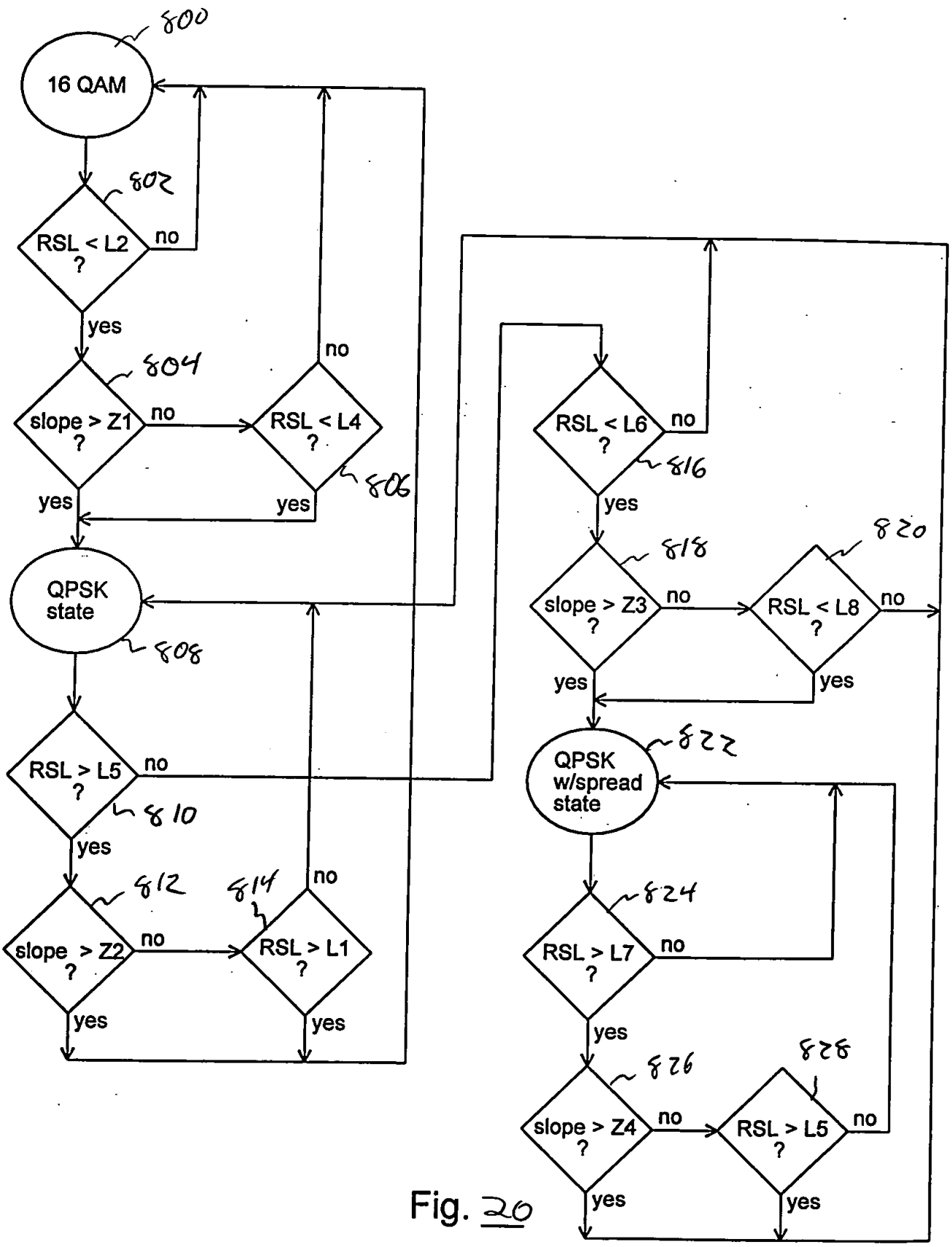

800
16 QAM
802
RSL < L2 ?
no
yes
804
slope > Z1 ?
no
RSL < L4 ?
no
806
yes
yes
QPSK state
808
RSL > L5 ?
no
810
yes
812
slope > Z2 ?
no
814
RSL > L1 ?
no
yes
yes
RSL < L6 ?
no
816
yes
818
slope > Z3 ?
no
820
RSL < L8 ?
no
yes
yes
822
QPSK w/spread state
824
RSL > L7 ?
no
yes
826
slope > Z4 ?
no
828
RSL > L5 ?
no
yes
yes

Fig. 20

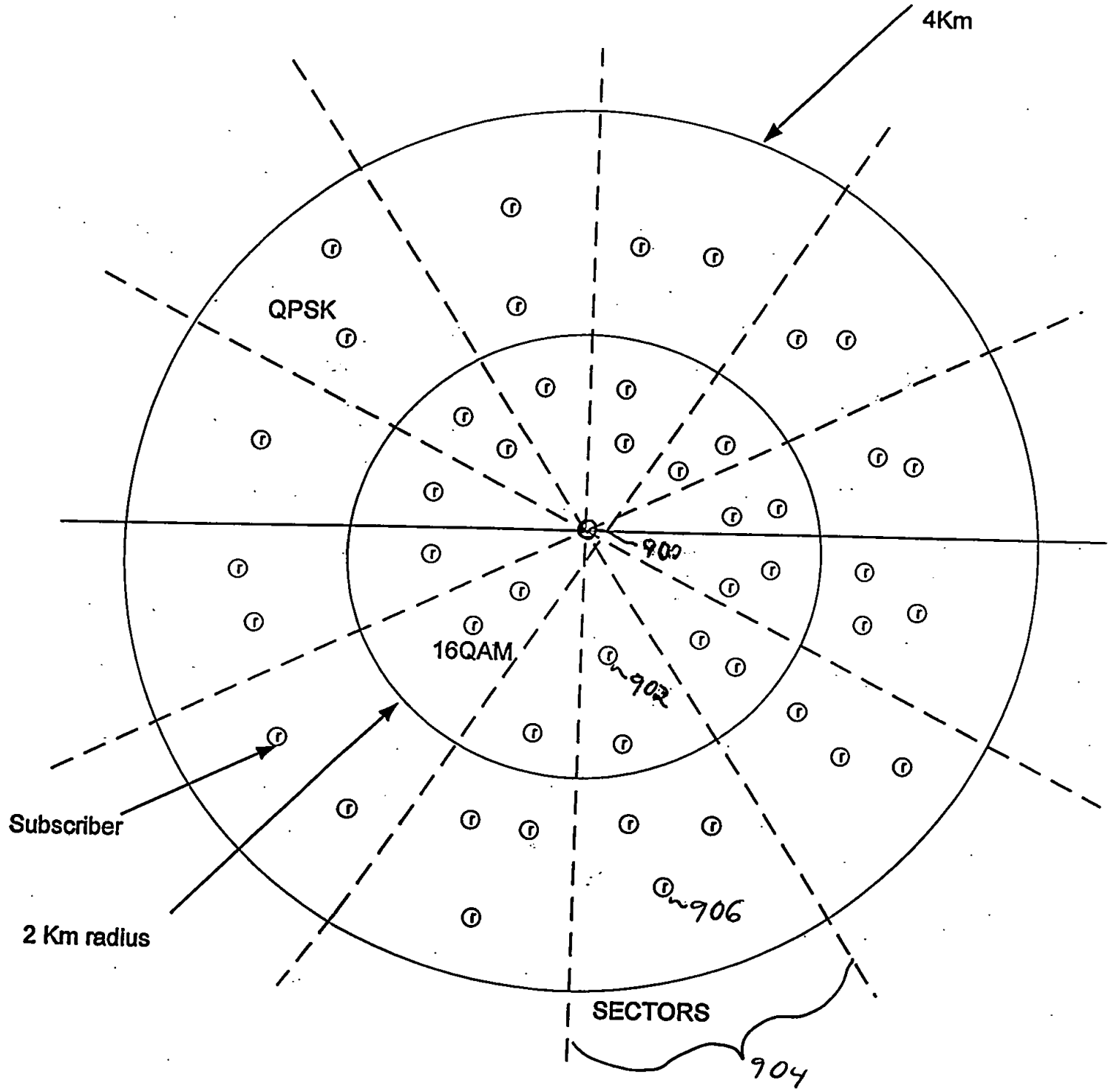

4Km
QPSK
16QAM
900
902
906
904
SECTORS
Subscriber
2 Km radius

Fig. 21

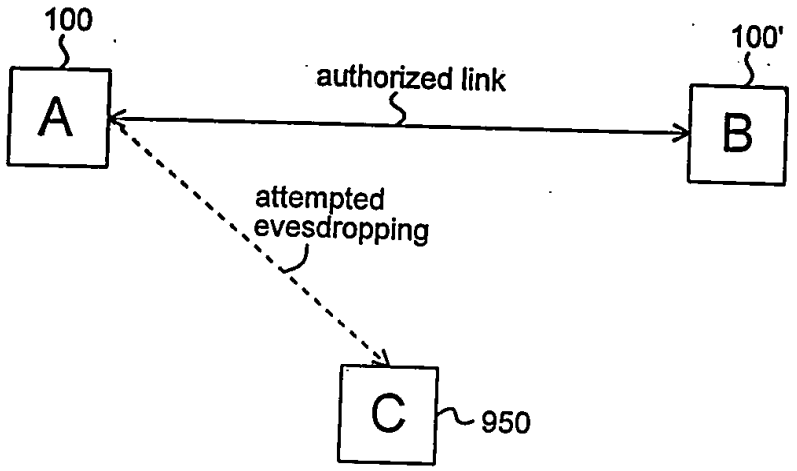


Fig. 22

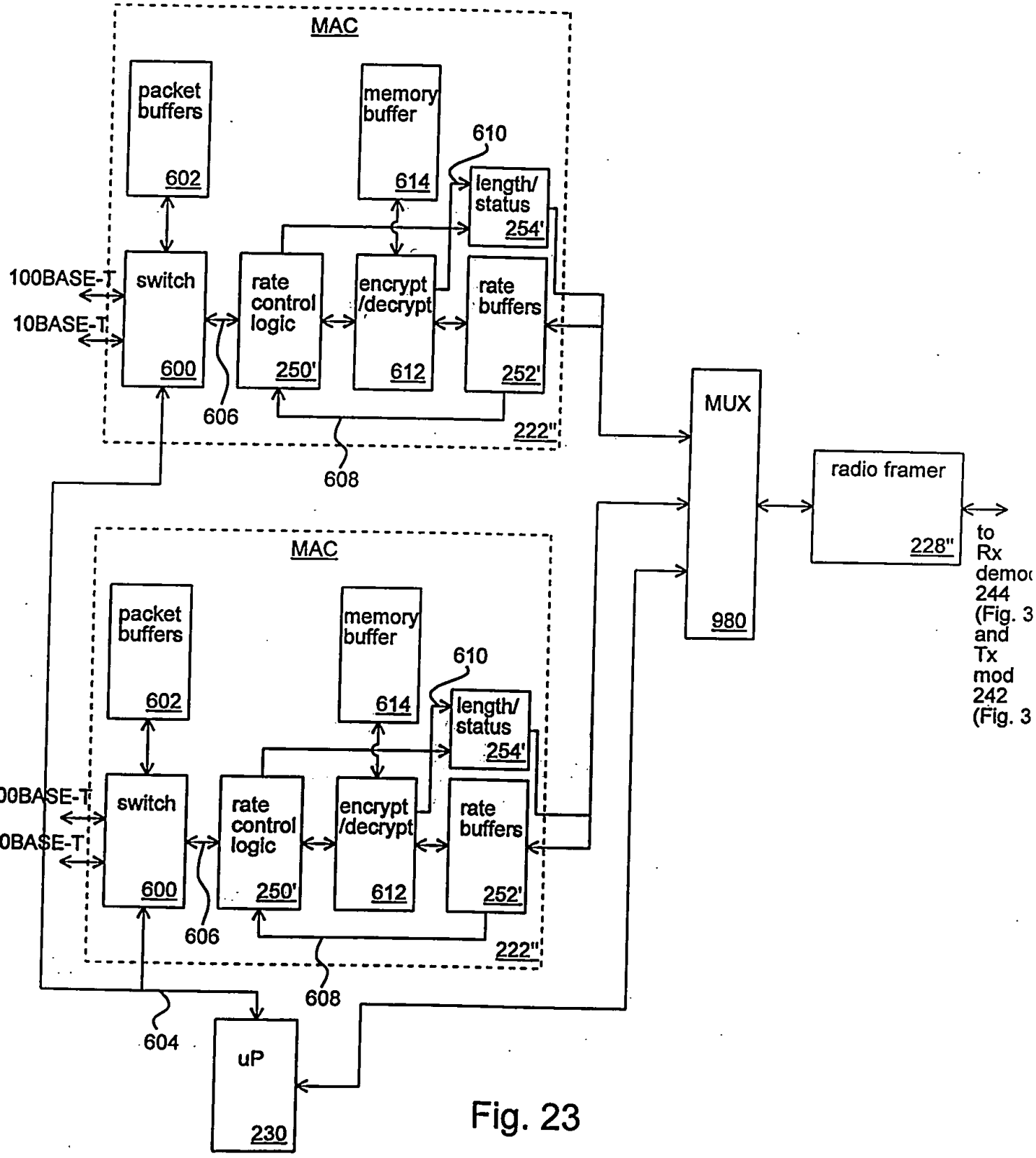

MAC
packet buffers
602
memory buffer
614
610
length/ status
254'
100BASE-T
10BASE-T
switch
600
rate control logic
250'
encrypt /decrypt
612
rate buffers
252'
606
222"
608
MUX
radio framer
228"
to Rx demod 244 (Fig. 3
and Tx mod 242 (Fig. 3
980
MAC
packet buffers
602
memory buffer
614
610
length/ status
254'
100BASE-T
10BASE-T
switch
600
rate control logic
250'
encrypt /decrypt
612
rate buffers
252'
606
222"
608
604
uP
230

Fig. 23